REMARKS

In the July 30, 2003 Final Office Action, the Examiner rejects Claims 1-15 and 18-22 under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,936,274 to Forbes et al. ("the Forbes patent") in view of U.S. Publication No. 2002/0142546 to Kouznetsov et al. ("the Kouznetsov application") and U.S. Patent No. 6,580,124 to Cleeves et al. ("the Cleeves patent"). The Examiner also rejected Claims 16-17 as obvious over the Forbes patent in view of the Kouznetsov application, the Cleeves patent and U.S. Patent No. 5,510,730 to El Gamal et al. ("the El Gamal patent").

I. REJECTION OF CLAIMS 1-15 AND 18-22 UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 1-15 and 18-22 as obvious over the Forbes patent in view the Kouznetsov application and the Cleeves patent. In view of the following discussion, Applicant respectfully traverses this rejection.

A. Claim 1

Focusing in particular on Claim 1 and the embodiment shown in Figure 11, a floating gate transistor 205 is disclosed having a pillar of semiconductor material 300 that extends outwardly from a working surface of a substrate 305 to form a source region 310, a body region 320 and a drain region 315. The floating gate transistor 205 includes a floating gate 202 along one side of the pillar 300, wherein the floating gate 202 overlaps the body region 320 in a horizontal direction. The floating gate transistor 205 further includes a control gate 335 overlaying the floating gate 202.

Since the floating gate 202 overlaps the body region 320 in the horizontal direction and the control gate 335 is placed above the floating gate 202, the control gate 335 has no overlap or alignment with the body region 320 in either the vertical direction or the horizontal direction. In contrast, the Forbes patent, the Kouznetsov application and the Cleeves patent disclose transistors with control gates that overlap or align with body regions.

Referring to Figure 3A of the Forbes patent, the Forbes patent discloses a floating gate transistor 205 with a control gate 335 adjacent to a floating gate 325, which is adjacent to a body region 320. Thus, the Forbes patent discloses a floating gate transistor with the control gate overlapping the body region in the horizontal direction.

Referring to Figure 8 (which is a side cross-sectional view from Figure 7) of the Kouznetsov application, the Kouznetsov application discloses a floating gate transistor with a control gate 43 above a floating gate 49, which is above a body region (also known as a channel island region 19). The Kouznetsov application suggests that a "fully aligned cell structure increases memory density and decreases die size and cost." See Paragraph No. [0024]. The specification of the Kouznetsov application states that the "first 55 and second 56 side surfaces of the control gate 43 are aligned to third 59 and fourth 61 side surfaces of the channel island region 19, and to third 63 and the fourth 65 side surfaces of the floating gate 49, as shown in FIG.8." See Paragraph No. [0056]. Thus, the Kouznetsov application teaches away from the claimed invention in that the Kouznetsov application teaches alignment of the control gate 43 to the channel island (or body) region 19 in the vertical direction.

Referring to Figures 1a and 1b (which are isometric views of a multigate transistor produced in accordance with a method illustrated by Figures 2a-2r) of the Cleeves patent, the Cleeves patent discloses a multigate transistor with control gates 118, 119, 120, 121 adjacent to charge storage mediums 114-117, which are formed on the sides of a body region 106. Thus, the Cleeves patent discloses a multigate transistor with control gates overlapping the body region in the horizontal direction.

Each of the references cited by the Examiner teaches transistors with control gates that overlap or align with body regions. Thus, the cited references do not disclose, teach or suggest a floating gate transistor with a control gate 335 that has no overlap or alignment with the body region 320 in either the vertical direction or the horizontal direction. Applicant therefore respectfully submits that Claim 1 is patentably distinguished over the cited references and Applicant respectfully requests allowance of Claim 1.

B. Claims 2-8

Claims 2-8, which depend from Claim 1, are believed to be patentable for the same reasons articulated above with respect to Claim 1, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claims 2-8.

C. Claim 9

Claim 9 is directed to an array of floating gate transistors with a plurality of semiconductor stacks arranged in rows and in columns, wherein each stack forms source, body, and drain regions of a respective floating gate transistor. A plurality of floating gates are in trenches between the columns of semiconductor stacks, wherein the floating gates are separated from respective sides of the semiconductor stacks by a gate dielectric. A plurality of control gates overlay the respective floating gates and are separated from the respective floating gates by an integrate dielectric.

Since the floating gates are in trenches between the columns of semiconductor stacks with body regions, there is overlap between the floating gates and the body regions in a horizontal direction. The control gates overlay the floating gates and do not overlap or align with the body regions.

In contrast, each of the cited references teaches transistors with control gates that overlap or align with body regions. In particular, the Forbes patent discloses floating gate transistors with control gates overlapping body regions in the horizontal direction. The Kouznetsov application discloses floating gate transistors with control gates aligned to body (or channel island) regions in the vertical direction. The Cleeves patent discloses multigate transistors with control gates overlapping body regions in the horizontal direction.

Therefore, the cited references do not disclose, teach or suggest an array of floating gate transistors with control gates that do not overlap or align with body regions. Accordingly, Applicant believes that Claim 9 is patentable over the cited references and Applicant respectfully requests allowance of Claim 9.

D. Claims 10-15 and 18-19

Claims 10-15 and 18-19, which depend from Claim 9, are believed to be patentable for the same reasons articulated above with respect to Claim 9, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claims 10-15 and 18-19.

E. Claim 20

Claim 20 is directed to a floating gate transistor that is fabricated upon a substrate. The floating gate transistor includes a first conductivity type semiconductor pillar formed upon the substrate, wherein the pillar has top and side surfaces. A first source/drain region of a second conductivity type forms in a portion of the pillar that is proximal to an interface between the pillar and the substrate. A second source/drain region of a second conductivity type forms in a portion of the pillar that is distal to the substrate and separated from the first source/drain region. A gate dielectric forms on at least a portion of one side surface of the pillar.

A floating gate is substantially adjacent a body region defined by the separation between the first source/drain region and the second source/drain region, wherein the floating gate is separated from the body region by the gate dielectric. An intergate dielectric forms on a top surface of the floating gate. A control gate substantially overlays the floating gate and is insulated from the floating gate by the intergate dielectric.

Since the floating gate is adjacent to the body region and the control gate overlays the floating gate, the control gate has no overlap or alignment with the body region. In contrast, the references cited by the Examiner disclose transistors with control gates that overlap or align with body regions.

In particular, the Forbes patent discloses a floating gate transistor with the control gate overlapping the body region in the horizontal direction. The Kouznetsov application teaches alignment of the control gate to the channel island (or body) region in the vertical direction. The Cleeves patent discloses a multigate transistor with control gates overlapping the body region in the horizontal direction.

Thus, the cited references do not teach, disclose or suggest a floating gate transistor with a control gate that does not overlap or align with the body region. Applicant therefore respectfully submits that Claim 20 is patentably distinguished over the cited references and Applicant respectfully requests allowance of Claim 20.

F. Claims 21-22

Claims 21-22, which depend from Claim 20, are believed to be patentable for the same reasons articulated above with respect to Claim 20, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claims 21-22.

II. REJECTION OF CLAIMS 16-17 UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 16-17 under 35 U.S.C. § 103(a) as being obvious over the Forbes patent in view of the Kouznetsov application, the Cleeves patent and the El Gamal patent. In view of the above discussion, Applicant respectfully traverses this rejection.

Claims 16-17, which depend from Claim 9, are believed to be patentable for the same reasons articulated above with respect to Claim 9, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claims 16-17.

III. CONCLUSION

In view of the foregoing, the present application is believed to be in condition for allowance, and such allowance is respectfully requested. If further issues remain to be resolved, the Examiner is cordially invited to contact the undersigned such that any remaining issues may be promptly resolved. Also, please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 9/30/03

By: Sharon S. Ng

Sharon S. Ng
Registration No. 53,383
Attorney of Record
Customer No. 20,995
(949) 760-0404

SSN-2578.DOC
092503